WHAT IS CLAIMED IS:

1. A method of delaying a clock signal for a multiple-data-rate interface comprising:

receiving a first edge of a first clock signal;

generating a first edge of a second clock signal by delaying the first clock signal by a first duration;

receiving a next edge of the first clock signal and the first edge of the second clock signal, the next edge of the first clock signal following the first edge of the first clock signal;

receiving a third clock signal;

generating a fourth clock signal by delaying the third clock signal by a second duration; and

increasing the first and second durations if the first edge of the second clock signal is received before the next edge of the first clock signal, else decreasing the first and second durations.

2. The method of claim 1 further comprising:

storing a data signal when the fourth clock signal transitions from a first logic level to a second logic level, and storing the data signal when the fourth clock signal transitions from the second logic level to the first logic level.

3. The method of claim 1 wherein the second duration is approximately equal to one-quarter the first duration.

4. The method of claim 1 wherein the multiple-data-rate interface is a double-data-rate interface.

5. The method of claim 1 wherein next edge of the first clock follows the first edge of the first clock by a clock cycle of the first clock.

6. A method of delaying a clock signal for a multiple-data-rate interface comprising:

receiving a first edge of a first clock signal;

generating a first edge of a second clock signal by delaying the first clock signal by a first duration and dividing the frequency of the first clock signal;

receiving a next edge of the first clock signal and the first edge of the second clock signal, the next edge of the first clock signal following the first edge of the first clock signal;

receiving a third clock signal;

generating a fourth clock signal by delaying the third clock signal by a second duration; and

increasing the first and second durations if the first edge of the second clock signal is received before the next edge of the first clock signal, else decreasing the first and second durations.

7. The method of claim 6 further comprising:

storing a data signal when the fourth clock signal transitions from a first logic level to a second logic level, and storing the data signal when the fourth clock signal transitions from the second logic level to the first logic level.

8. The method of claim 6 wherein the second duration is approximately equal to one-quarter the first duration.

9. The method of claim 6 wherein the multiple-data-rate interface is a double-data-rate interface.

10. The method of claim 6 wherein next edge of the first clock follows the first edge of the first clock by a clock cycle of the first clock.

11. The method of claim 6 wherein the first clock signal is divided in frequency then delayed by the first duration.

12. The method of claim 11 wherein the frequency of the first clock signal is divided in frequency by a value selected from the group consisting of 4, 8, and 16.

13. The method of claim 6 wherein the first clock signal is delayed by the first duration before its frequency is divided.

14. An integrated circuit comprising:

a series of circuits;

a phase detector having a first input coupled to an input of the series of circuits and a second input coupled to an output of the series of circuits;

an up/down counter having an input coupled to an output of the phase detector; and

a first variable-delay block having a control input coupled to an output of the up/down counter,

wherein the series of circuits comprises:

a second variable-delay block having a control input coupled to the output of the up/down counter; and

a frequency divider.

15. The integrated circuit of claim 14 further comprising:

a first flip-flop having a clock input coupled to an output of the first variable-delay block; and

a second flip-flop having a complementary clock input coupled to the output of the first variable-delay block.

16. The integrated circuit of claim 15 further comprising:

a third flip-flop coupled between the phase detector and the up/down counter.

17. The integrated circuit of claim 14 wherein an input of the second variable-delay block is coupled to an output of the frequency divider.

18. The integrated circuit of claim 14 wherein an output of the frequency divider is coupled to an input of the second variable-delay block.

19. An integrated circuit comprising:

a series combination of a first frequency divider and a first variable-delay block, configured to receive a first clock signal;

a phase detector configured to receive the first clock signal and an output from the series combination;

an up/down counter configured to receive an output from the phase detector; and

a second variable-delay block configured to receive a second clock signal,

wherein the first variable-delay block and the second variable-delay block are configured to receive an output from the up/down counter.

20. The integrated circuit of claim 19 wherein the first frequency divider is configured to receive the first clock signal and the first variable-delay block is configured to receive an output from the first frequency divider.

21. The integrated circuit of claim 19 wherein the first variable-delay block is configured to receive the first clock signal and the first frequency divider is configured to receive an output from the first variable-delay block.

22. The integrated circuit of claim 19 further comprising:

a first flip-flop having a clock input configured to receive an output of the first variable-delay block; and

a second flip-flop having a complementary clock input configured to receive the output of the first variable-delay block.

23. The integrated circuit of claim 22 further comprising:

a memory configured to receive an output of the first flip-flop and an output of the second flip-flop.

24. The integrated circuit of claim 22 further comprising:

an synchronous dynamic random access memory configured to receive an output of the first flip-flop and an output of the second flip-flop.

25. The integrated circuit of claim 19 further comprising:

a third flip-flop coupled between the phase detector and the up/down counter.

26. The integrated circuit of claim 25 further comprising:

a second frequency divider configured to receive the first clock signal to provide a third clock signal to the up/down counter.

27. The integrated circuit of claim 19 wherein the integrated circuit is a programmable logic device.

28. A computing system comprising:

a multiple-data-rate memory; and

the integrated circuit of claim 14 coupled to the multiple-data-rate memory.

29. The computing system of claim 28 wherein the multiple-data-rate memory is a double-data-rate memory.

30. An integrated circuit comprising:

a series of circuits comprising:

a dividing means for dividing a frequency of a clock signal; and

a first delaying means for delaying a clock signal by a first duration,

wherein the series of circuits receives a first clock signal and provides a second clock signal, the second clock signal delayed and divided in frequency from the first clock signal;

phase detector means for receiving the first and second clock signals, and providing an output;

a second delaying means for delaying a third clock signal by a second duration; and

adjustment means for increasing or decreasing the first and second durations based on the output of the phase detector means.

31. The integrated circuit of claim 30 wherein the series of circuits provides the second clock signal by first dividing the frequency of the first clock signal.

32. The integrated circuit of claim 31 wherein the frequency of the first clock signal is divided by a value selected from the group consisting of 4, 8, and 16.

33. The integrated circuit of claim 30 wherein the series of circuits provides the second clock signal by delaying the first clock signal before dividing its frequency.